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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/020,426	12/07/2001	Daniel M. Castagnozzi	applied_114	9539

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EXAMINER	
TORRES, JOSEPH D	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 03/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/020,426	CASTAGNOZZI ET AL.	
	Examiner	Art Unit	
	Joseph D. Torres	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 February 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *17-48* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *17-48* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 February 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings were received on 02/14/2005. These drawings are accepted.

Claim Rejections - 35 USC § 112

2. In view of the Amendment filed 02/14/2005, the Examiner withdraws the 35 USC § 112 rejections of the previous Office Action.

Response to Arguments

3. Applicant's arguments filed 02/14/2005 have been fully considered but they are not persuasive.

The Applicant contends, "The hard-limited signal is not the same as the Applicant's bit estimate, because a bit estimate is a preliminary judgment of a symbol value (a '0' or a '1'). Despite the fact that Andresen's hard-limited signal assumes a binary format in most situations, it is not treated as binary data, but merely a step in signal processing. It is not binary data because Andresen makes no attempt to determine symbol values until much later in the process, after signal processing in the Data Detector".

The Examiner disagrees and asserts that even the Abstract in Andresen teaches that the circuitry in Andresen is for resolving an analog signal representing binary data into its binary format. The sole purpose of the circuitry in Andresen is to provide preliminary

judgments, i.e., estimates, on the analog signal representing binary data in order to resolve the analog signal representing binary data into binary digital data format.

The Applicant contends, "The Office Action (page 6) states that 'bit value reference decisions R1 and R2 are predetermined reference values made across a plurality of clock cycles'. However, R1 and R2 are merely dc voltages. The constant amplitude voltage levels associated with R1 and R2 can be clearly seen in Fig. 7. Data values that are determined in non-current clock cycles are never introduced into Andresen's data detector 28".

The Examiner asserts that the previous claim language "the non-casual circuit comparing a current bit estimate to bit value decisions made across a plurality of clock cycles" has been eliminated from claim 17.

Claim 17 now recites "an output to supply a first bit value for a current clock cycle in response to comparing a first bit estimate for the current clock cycle, to bit values determined in a non-current clock cycle".

The Examiner asserts that Exclusive OR circuit 112 in Figure 6 of Andresen is substantially a comparator since it provides a 1 if input signal match and a 0 if they do not match. Exclusive OR circuit 112 in Figure 6 receives a current bit estimate A and a previous bit estimate A from Delay 110 in Figure 6. Previous bit estimate A from Delay 110 in Figure 6 is a bit value for a non-current clock cycle. Hence Andresen teaches an output DATA in Figure 1 of Andresen to supply a first bit value for a current clock cycle in response to comparing a first bit estimate A for the current clock cycle, to bit values

determined A from Delay 110 in Figure 6 in a non-current clock cycle (Note Figure 6 is the Data Detector 28 of Figure 1 in Andresen).

The Applicant contends, "Even if an expert were motivated to reduce the numbers of errors in Andresen's system, there appears to be no motivation to use any particular modulation format, such as NRZ, to accomplish this task".

In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, NRZ is primarily designed for magnetic media and is a means whereby a pulse is recorded on magnetic tape by polarity reversal. The IEEE Authoritative Dictionary of IEEE Standards Terms defined NRZ as a "method whereby a pulse is recorded on the magnetic tape by polarity reversal of the recording head current". Even the IEEE Authoritative Dictionary of IEEE Standards Terms recognizes that the primary usefulness for NRZ is for magnetic recording media.

The Applicant contends, "With respect to the second prima facie obviousness requirement, even if the references are combined, there is no reasonable expectation of success".

The Examiner disagrees and asserts that the circuit in Andresen is designed to resolve an analog received signal representing binary data into binary digital data format. In that binary format is NRZ binary data format, the circuit in Andresen will not require any modification to resolve the analog signal representing NRZ binary data into NRZ binary digital data format. The Abe Prior art was introduced solely to show that NRZ is well known in the Prior Art and widely used. The circuitry in the Andresen patent need no part of the circuitry in the Abe patent for resolving the analog signal representing NRZ binary data into NRZ binary digital data format.

The Applicant contends, "Applicant notes that the '332 application was filed after the instant application. Further, the '332 application was filed as a CIP of the instant application. Therefore, a terminal disclaimer seems unnecessary".

The Examiner asserts that the proper way to overcome a nonstatutory double patenting rejection is through the filing of a terminal disclaimer.

The Examiner disagrees with the applicant and maintains all rejections of claims 17-48. All amendments and arguments by the applicant have been considered. It is the Examiner's conclusion that claims 17-48 are not patentably distinct or non-obvious over the prior art of record in view of the references, Andresen; Rolf et al. (US 3670304 A) in

view of Abe; Katsuaki et al. (US 5781588 A, hereafter referred to as Owaki) as applied in the last office action, filed 12/09/2004. Therefore, the rejection is maintained.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. Claims 17, 33 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Andresen; Rolf et al. (US 3670304 A) in view of Abe; Katsuaki et al. (US 5781588 A, hereafter referred to as Owaki).

35 U.S.C. 103(a) rejection of claims 17 and 33.

Andresen teaches a multi-threshold decision circuit having an input to accept a data stream encoded with forward error correction FEC (Amplitude Sense and Data Gates 20 in Figures 1 & 3 in Andresen are a multi-threshold decision circuit having an input to

accept a data stream encoded with forward error correction FEC), an input to accept threshold values (Input Line 44 in Figure 1 of Andresen provides a Change Threshold value to Amplitude Sense and Data Gates 20), and outputs to provide bit estimates responsive to a plurality of voltage threshold levels (Output Lines 27 and 72 in Figures 1 & 3 of Andresen provide bit estimates responsive to a plurality of voltage threshold levels); a non-casual circuit having inputs to accept bit estimates from the multi-threshold decision circuit (Data/Error Detectors in Figures 1 & 3 of Andresen are a non-causal circuit having inputs to accept bit estimates from the Amplitude Sense and Data Gates multi-threshold decision circuit 20), the non-casual circuit comparing a current bit estimate to bit value decisions made across a plurality of clock cycles (non-casual circuit Data/Error Detectors in Figures 1 & 3 of Andresen comprise Data Detector 28 in Figure 1 & 6 comprising Comparators 124 & 138 in Figure 6 for comparing a current bit estimate D in Figures 6 & 7 to bit value reference decisions R1 and R2 made across a plurality of clock cycles; Note: bit value reference decisions R1 and R2 are predetermined reference values made across a plurality of clock cycles); the non-casual circuit having an output to supply a bit value for the current bit estimate determined in response to the non-casual bit value comparisons (Data Detector 28 inside the non-casual circuit Data/Error Detectors 24 in Figures 1 & 3 of Andresen supplies a Data output which is the current bit estimate determined in response to the non-casual bit value comparisons); a forward error correction FEC circuit having an input to receive the first bit value from the non-casual circuit (Parity Check Circuit 94 and Error Correction Circuit 96 in Figure 3 of Andresen are an FEC circuit having an

input to receive a first bit value from the non-casual circuit Data/Error Detectors 24), the FEC circuit decoding the incoming data stream and correcting bit values in response to the decoding (the FEC circuit Parity Check Circuit 94 and Error Correction Circuit 96 in Figure 3 of Andresen decode and correct the incoming data stream), the FEC circuit having an output to supply a stream of corrected data bits (the FEC circuit Parity Check Circuit 94 and Error Correction Circuit 96 in Figure 3 of Andresen have an output to supply the Read Data stream of corrected data bits); and, a statistics circuit having an input to accept the first bit value from the non-casual circuit, an input to accept the stream of corrected data bits from the FEC circuit, and an output to supply threshold values to the multi-threshold circuit in response to analysis of the FEC error statistics (Check Change Threshold Circuits 26, 90 and 92 in Figures 1 & 3 of Andresen are a statistics circuit having an input to accept the first bit value from the non-casual circuit Data/Error Detectors 24, an input to accept the stream of corrected data bits from the FEC circuit Parity Check Circuit 94 and Error Correction Circuit 96, and an output to supply threshold values to the multi-threshold circuit Amplitude Sense and Data Gates 20 in Figures 1 & 3 in response to analysis of the FEC error statistics).

The Examiner asserts that Exclusive OR circuit 112 in Figure 6 of Andresen is substantially a comparator since it provides a 1 if input signal match and a 0 if they do not match. Exclusive OR circuit 112 in Figure 6 receives a current bit estimate A and a previous bit estimate A from Delay 110 in Figure 6. Previous bit estimate A from Delay 110 in Figure 6 is a bit value for a non-current clock cycle. Hence Andresen teaches an output DATA in Figure 1 of Andresen to supply a first bit value for a current clock cycle

in response to comparing a first bit estimate A for the current clock cycle, to bit values determined A from Delay 110 in Figure 6 in a non-current clock cycle (Note Figure 6 is the Data Detector 28 of Figure 1 in Andresen).

However Andresen does not explicitly teach the specific use of non-return to zero NRZ. Abe, in an analogous art, teaches use of non-return to zero NRZ (see Col. 23, lines 42-46, Abe). Note: the circuit in Andresen is designed to resolve and reproduce digital data and NRZ encoded data is digital data; hence it would be obvious to apply the teachings in the Andresen patent to a specific type of data for which it was designated such as NRZ which is a widely used form of encoding for magnetic storage devices.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Andresen with the teachings of Abe by including use of non-return to zero NRZ. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of non-return to zero NRZ would have provided the opportunity to apply the teachings in the Andresen patent to a specific type of data for which it was designated such as NRZ which is a widely used form of encoding for magnetic storage devices in order to equalize BER's for respective different symbol states (col. 36, lines 27-29 in Abe).

35 U.S.C. 103(a) rejection of claim 35.

Andresen teaches a multi-threshold decision circuit having an input to accept a data stream encoded with forward error correction FEC (Amplitude Sense and Data Gates

20 in Figures 1 & 3 in Andresen are a multi-threshold decision circuit having an input to accept a data stream encoded with forward error correction FEC), an input to accept threshold values (Input Line 44 in Figure 1 of Andresen provides a Change Threshold value to Amplitude Sense and Data Gates 20), and outputs to provide bit estimates responsive to a plurality of voltage threshold levels (Output Lines 27 and 72 in Figures 1 & 3 of Andresen provide bit estimates responsive to a plurality of voltage threshold levels); a non-casual circuit having inputs to accept bit estimates from the multi-threshold decision circuit (Data/Error Detectors in Figures 1 & 3 of Andresen are a non-causal circuit having inputs to accept bit estimates from the Amplitude Sense and Data Gates multi-threshold decision circuit 20), the non-casual circuit comparing a current bit estimate to bit value decisions made across a plurality of clock cycles (non-casual circuit Data/Error Detectors in Figures 1 & 3 of Andresen comprise Data Detector 28 in Figure 1 & 6 comprising Comparators 124 & 138 in Figure 6 for comparing a current bit estimate D in Figures 6 & 7 to bit value reference decisions R1 and R2 made across a plurality of clock cycles; Note: bit value reference decisions R1 and R2 are predetermined reference values made across a plurality of clock cycles); the non-casual circuit having an output to supply a bit value for the current bit estimate determined in response to the non-casual bit value comparisons (Data Detector 28 inside the non-casual circuit Data/Error Detectors 24 in Figures 1 & 3 of Andresen supplies a Data output which is the current bit estimate determined in response to the non-casual bit value comparisons); a forward error correction FEC circuit having an input to receive the first bit value from the non-casual circuit (Parity Check Circuit 94

and Error Correction Circuit 96 in Figure 3 of Andresen are an FEC circuit having an input to receive a first bit value from the non-casual circuit Data/Error Detectors 24), the FEC circuit decoding the incoming data stream and correcting bit values in response to the decoding (the FEC circuit Parity Check Circuit 94 and Error Correction Circuit 96 in Figure 3 of Andresen decode and correct the incoming data stream), the FEC circuit having an output to supply a stream of corrected data bits (the FEC circuit Parity Check Circuit 94 and Error Correction Circuit 96 in Figure 3 of Andresen have an output to supply the Read Data stream of corrected data bits); and, a statistics circuit having an input to accept the first bit value from the non-casual circuit, an input to accept the stream of corrected data bits from the FEC circuit, and an output to supply threshold values to the multi-threshold circuit in response to analysis of the FEC error statistics (Check Change Threshold Circuits 26, 90 and 92 in Figures 1 & 3 of Andresen are a statistics circuit having an input to accept the first bit value from the non-casual circuit Data/Error Detectors 24, an input to accept the stream of corrected data bits from the FEC circuit Parity Check Circuit 94 and Error Correction Circuit 96, and an output to supply threshold values to the multi-threshold circuit Amplitude Sense and Data Gates 20 in Figures 1 & 3 in response to analysis of the FEC error statistics).

The Examiner asserts that Exclusive OR circuit 112 in Figure 6 of Andresen is substantially a comparator since it provides a 1 if input signal match and a 0 if they do not match. Exclusive OR circuit 112 in Figure 6 receives a current bit estimate A and a previous bit estimate A from Delay 110 in Figure 6. Previous bit estimate A from Delay 110 in Figure 6 is a bit value for a non-current clock cycle. Hence Andresen teaches an

output DATA in Figure 1 of Andresen to supply a first bit value for a current clock cycle in response to comparing a first bit estimate A for the current clock cycle, to bit values determined A from Delay 110 in Figure 6 in a non-current clock cycle (Note Figure 6 is the Data Detector 28 of Figure 1 in Andresen).

However Andresen does not explicitly teach the specific use of non-return to zero NRZ or the use of FEC error statistics to set the threshold.

Abe, in an analogous art, teaches use of non-return to zero NRZ (see Col. 23, lines 42-46, Abe). Note: the circuit in Andresen is designed to resolve and reproduce digital data and NRZ encoded data is digital data; hence it would be obvious to apply the teachings in the Andresen patent to a specific type of data for which it was designated such as NRZ which is a widely used form of encoding for magnetic storage devices. Figure 37 of Abe teaches BER CALC circuit for producing error statistics for use in threshold adjusting circuit 2604. Note: Abe teaches that Figure 37 is a modification of Figure 33 in Abe using BER in order to equalize BER's for respective different symbol states (col. 36, lines 27-29 in Abe).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Andresen with the teachings of Abe by including use of non-return to zero NRZ. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of non-return to zero NRZ would have provided the opportunity to apply the teachings in the Andresen patent to a specific type of data for which it was designated such as NRZ which is a widely used form of encoding for

magnetic storage devices in order to equalize BER's for respective different symbol states (col. 36, lines 27-29 in Abe).

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

5. Claims 17-48 are provisionally rejected under the judicially created doctrine of double patenting over claims 16-28 of copending Application No. 10/077,332. This is a provisional double patenting rejection since the conflicting claims have not yet been patented.

See the Non-Final Action filed 12/09/2004 for detailed action of prior rejections.

Conclusion

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

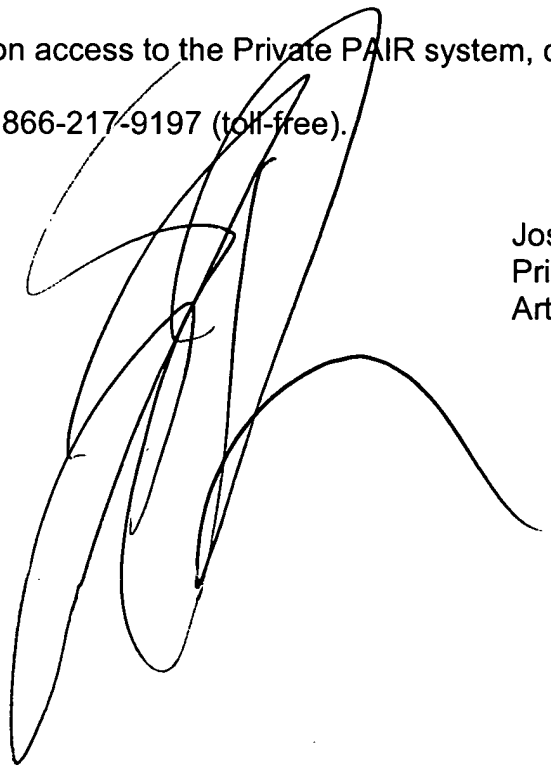
§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph D. Torres whose telephone number is (571) 272-3829. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



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